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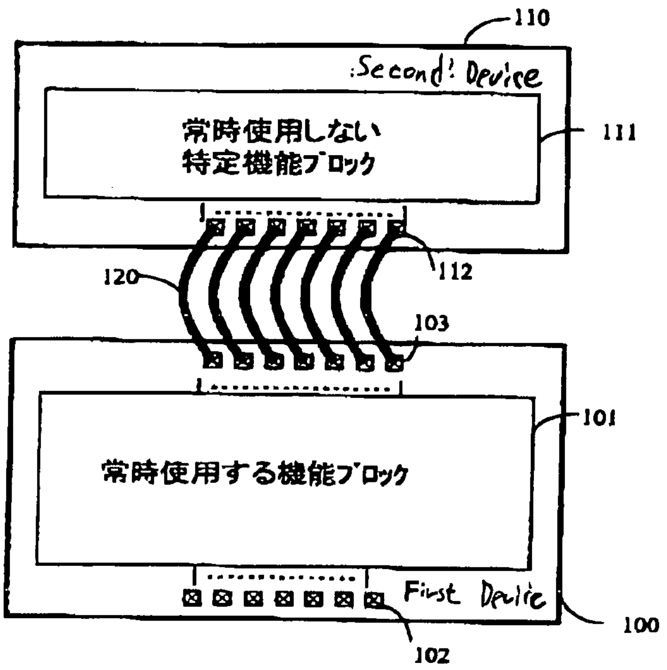
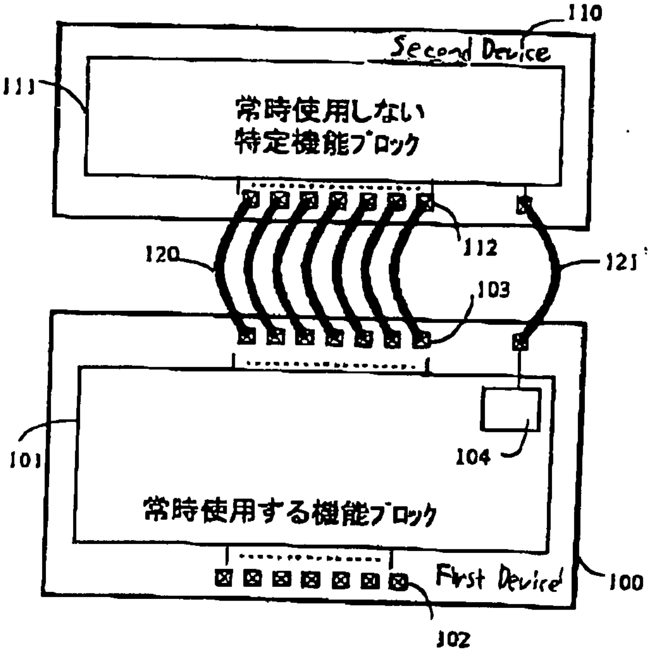
Fig. 1


110
Second Device
常時使用しない
特定機能ブロック
111
112
120
103
常時使用する機能ブロック
101
First Device
100
102

100 常時使用しない特定機能ブロックを除いた半導体装置（第1の装置）
101 常時使用する機能ブロック
102 第1の装置の制御端子
103 制御バス端子
110 常時使用しない特定機能装置（第2の装置）
111 常時使用しない特定機能ブロック
112 制御バス端子
120 接続線

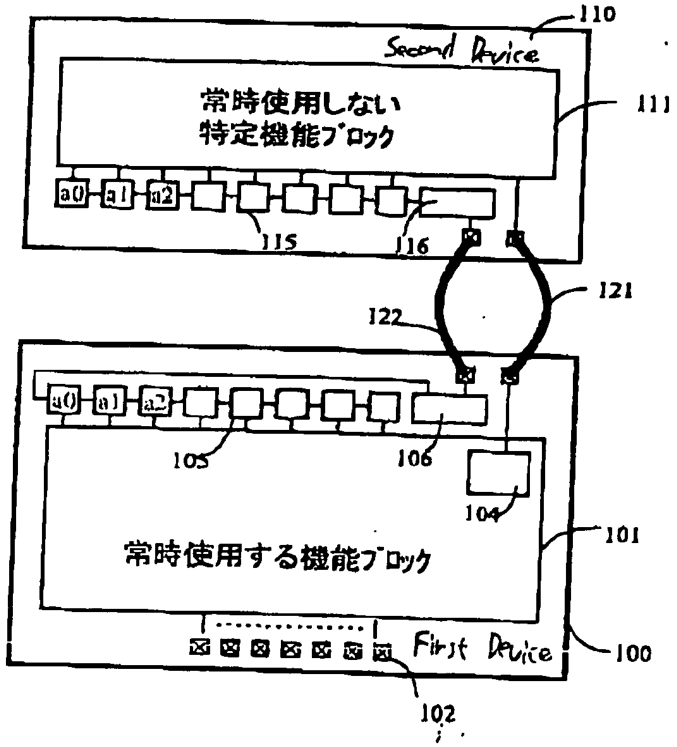
100: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
101: ALWAYS-USED FUNCTION BLOCK
102: CONTROL TERMINAL OF FIRST DEVICE
103: CONTROL BUS TERMINAL
110: DEVICE (SECOND DEVICE) HAVING NON-ALWAYS-USED PARTICULAR FUNCTION
111: NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
112: CONTROL BUS TERMINAL
120: CONNECTION LINE

Fig. 2


110
Second Device
111
常時使用しない
特定機能ブロック
112
120
121
103
101
104
常時使用する機能ブロック
First Device
100
102

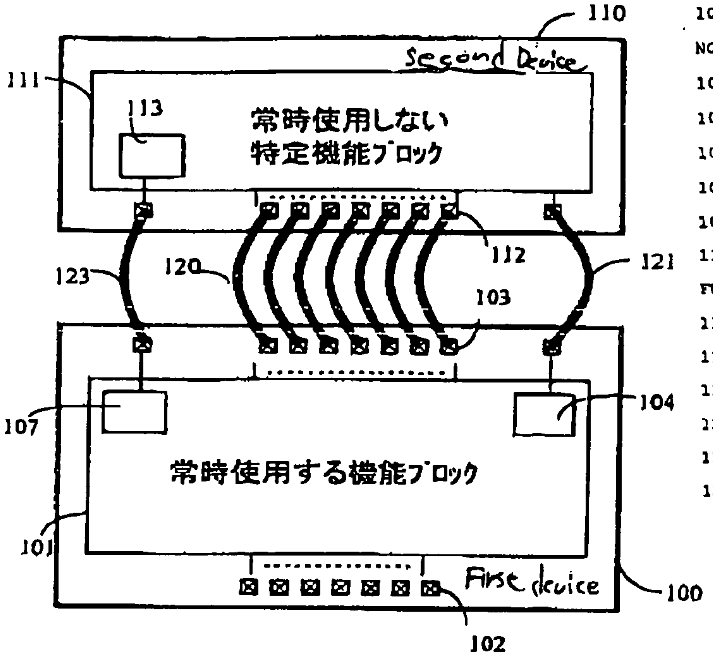
100: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
101: ALWAYS-USED FUNCTION BLOCK
102: CONTROL TERMINAL OF FIRST DEVICE
103: CONTROL BUS TERMINAL
104: SECOND DEVICE CONTROL START SIGNAL GENERATION CIR.
110: DEVICE (SECOND DEVICE) HAVING NON-ALWAYS-USED PARTICULAR FUNCTION
111: NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
112: CONTROL BUS TERMINAL
120: CONNECTION LINE
121: SECOND DEVICE CONTROL START SIGNAL LINE

Fig 3


110
Second Device
常時使用しない
特定機能ブロック
111
a0
a1
a2
115
116
121
122
a0
a1
a2
105
106
104
常時使用する機能ブロック
101
First Device
100
102

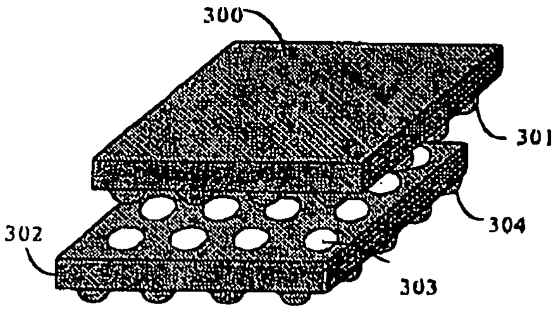
100: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
101: ALWAYS-USED FUNCTION BLOCK
102: CONTROL TERMINAL OF FIRST DEVICE
104: SECOND DEVICE CONTROL START SIGNAL GENERATION CIR.
105: CONTROL SIGNAL REGISTER GROUP OF FIRST DEVICE
106: SERIAL I/F OF FIRST DEVICE
110: DEVICE (SECOND DEVICE) HAVING NON-ALWAYS-USED PARTICULAR FUNCTION
111: NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
115: CONTROL SIGNAL REGISTER GROUP OF SECOND DEVICE
116: SERIAL I/F OF SECOND DEVICE
121: SECOND DEVICE CONTROL START SIGNAL LINE
122: SERIAL CONTROL SIGNAL LINE

Fig. 4


110
Second Device
111
113
常時使用しない
特定機能ブロック
112
123
120
103
121
107
104
常時使用する機能ブロック
101
First device
100
102

100: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
101: ALWAYS-USED FUNCTION BLOCK
102: CONTROL TERMINAL OF FIRST DEVICE
103: CONTROL BUS TERMINAL
104: SECOND DEVICE CONTROL START SIGNAL GENERATION CIR.
107: SECOND DEVICE DETECTION CIR.
110: DEVICE (SECOND DEVICE) HAVING NON-ALWAYS-USED PARTICULAR FUNCTION
111: NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
112: CONTROL BUS TERMINAL
113: IDENTIFICATION SIGNAL GENERATION CIR.
120: CONNECTION LINE
121: SECOND DEVICE CONTROL START SIGNAL LINE
123: SECOND DEVICE IDENTIFICATION SIGNAL LINE

Fig. 5


300
301
304
302
303

300: PACKAGE INCORPORATING SECOND DEVICE
301: BALL GRID ARRAY ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)
302: PACKAGE INCORPORATING FIRST DEVICE
303: PACKAGE CONTACT SURFACES OF PACKAGE INCORPORATING FIRST DEVICE (CONTROL BUS TERMINALS OF FIRST DEVICE)
304: BALL GRID ARRAY ELECTRODES OF PACKAGE INCORPORATING FIRST DEVICE (CONTROL TERMINALS OF FIRST DEVICE)

Fig. 6

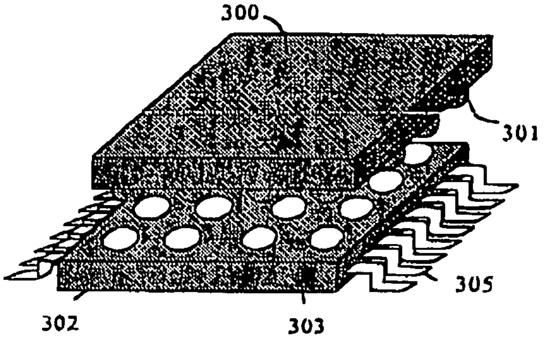
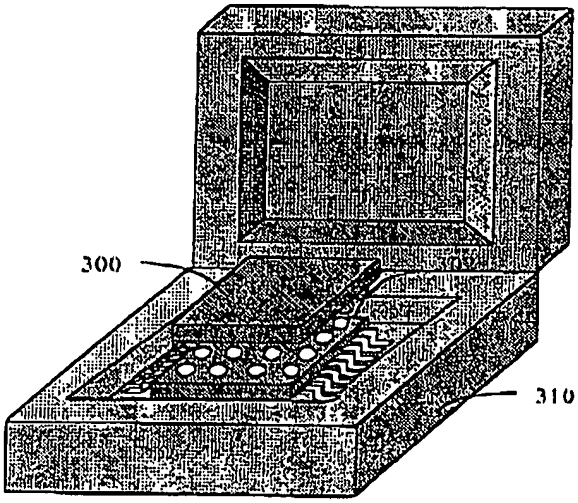
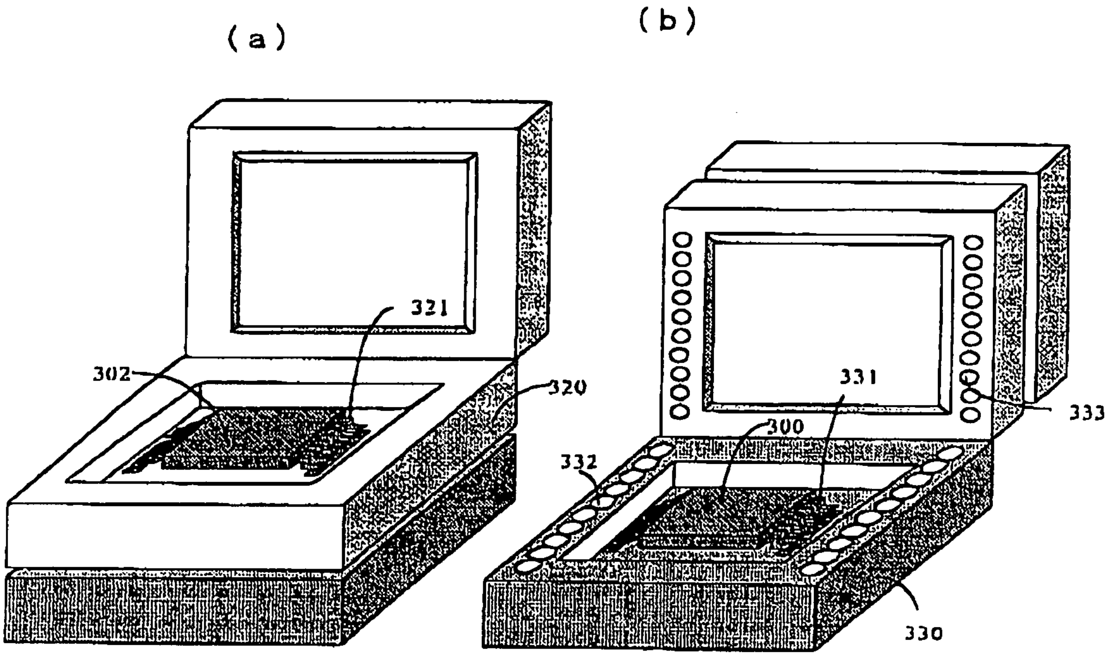

300
301
305
302
303

Fig. 7



300: PACKAGE INCORPORATING SECOND DEVICE
302: PACKAGE INCORPORATING FIRST DEVICE
310: SOCKET FOR CONNECTING TWO PACKAGES

Fig. 8



300: PACKAGE INCORPORATING SECOND DEVICE

302: PACKAGE INCORPORATING FIRST DEVICE

320: FIRST PACKAGE INSERTION PORTION OF 2-STAGE CONNECTION SOCKET

321: ELECTRODES OF PACKAGE INCORPORATING FIRST DEVICE (CONTROL BUS TERMINALS AND CONTROL TERMINALS OF FIRST DEVICE)

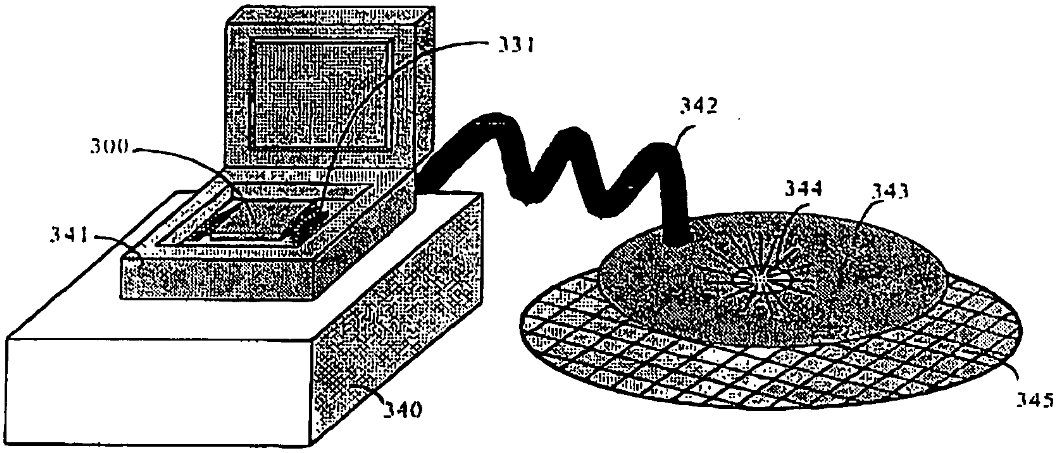
330: SECOND PACKAGE INSERTION PORTION OF 2-STAGE CONNECTION SOCKET

331: ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

332: CONNECTION SIGNAL ELECTRODES CONNECTED TO SECOND PACKAGE (CONTROL BUS TERMINALS OF SECOND DEVICE)

333: CONNECTION SIGNAL ELECTRODES CONNECTED TO FIRST PACKAGE (CONTROL BUS TERMINALS OF SECOND DEVICE)

Fig.9



300: PACKAGE INCORPORATING SECOND DEVICE

331: ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

340: APPARATUS (E.G., GENERAL-PURPOSE TESTING APPARATUS) FOR SETTING FUNCTION IN FIRST DEVICE

341: SOCKET IN WHICH SECOND PACKAGE IS INSERTED

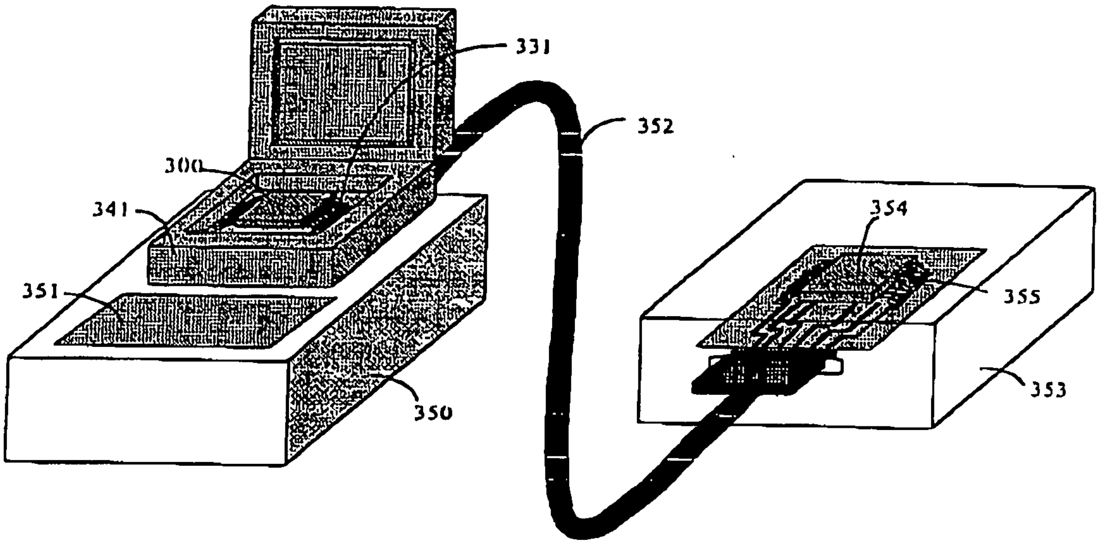
342: CONNECTION LINE (FOR CONTROL BUS TERMINALS SIGNALS FROM FIRST DEVICE AND CONTROL TERMINAL SIGNALS FROM SECOND DEVICE)

343: PROBE CARD

344: PROBE ELECTRODES (CONTROL BUS TERMINALS FOR FIRST DEVICE AND CONTROL TERMINALS FOR SECOND DEVICE)

345: WAFER ON WHICH FIRST DEVICES ARE FORMED

Fig. 10



300: PACKAGE INCORPORATING SECOND DEVICE

331: ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

341: SOCKET IN WHICH SECOND PACKAGE IS INSERTED

350: APPARATUS (E.G., GENERAL-PURPOSE REWRITING APPARATUS) FOR SETTING FUNCTIONS IN FIRST DEVICE

351: MANIPULATION SURFACE OF FUNCTION SETTING APPARATUS

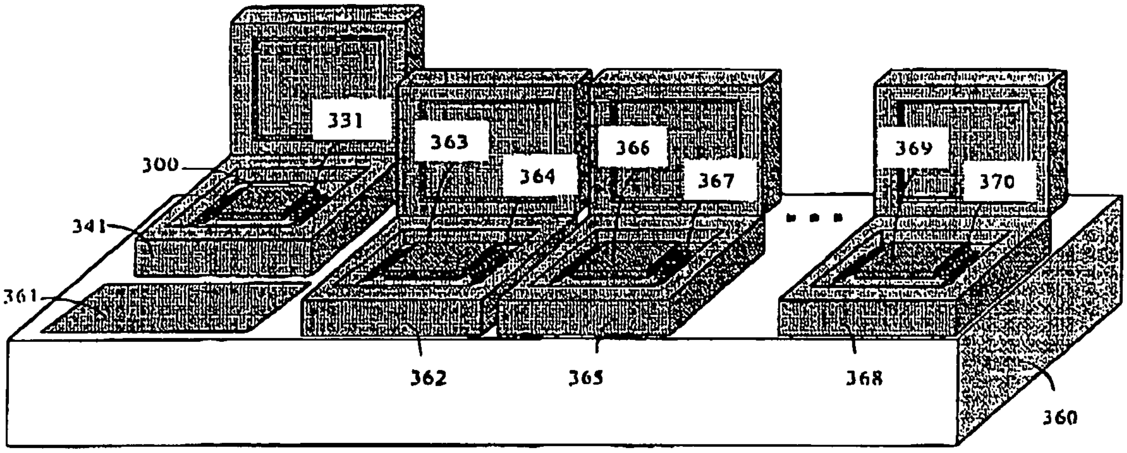
352: CONNECTION LINE (FOR CONTROL BUS TERMINALS SIGNALS FROM FIRST DEVICE AND CONTROL TERMINAL SIGNALS FROM SECOND DEVICE)

353: APPARATUS (E.G., CELLULAR PHONE) INCORPORATING FIRST DEVICE

354: PACKAGE INCORPORATING FIRST DEVICE

355: ELECTRODES OF PACKAGE INCORPORATING FIRST DEVICE (CONTROL BUS TERMINALS FOR FIRST DEVICE AND CONTROL TERMINALS FOR SECOND DEVICE)

Fig. 11



300: PACKAGE INCORPORATING SECOND DEVICE

331: ELECTRODES OF PACKAGE INCORPORATING SECOND DEVICE (CONTROL BUS TERMINALS OF SECOND DEVICE)

341: SOCKET IN WHICH SECOND PACKAGE IS INSERTED

360: APPARATUS (E.G., GENERAL-PURPOSE REWRITING APPARATUS) FOR SETTING FUNCTIONS IN FIRST DEVICE

361: MANIPULATION SURFACE OF FUNCTION SETTING APPARATUS

362: SOCKET IN WHICH FIRST FIRST PACKET IS INSERTED

363: PACKAGE INCORPORATING FIRST FIRST DEVICE

364: ELECTRODES OF PACKAGE INCORPORATING FIRST FIRST DEVICE (CONTROL BUS TERMINALS AND CONTROL TERMINALS OF FIRST DEVICE)

365: SOCKET IN WHICH SECOND FIRST PACKET IS INSERTED

366: PACKAGE INCORPORATING SECOND FIRST DEVICE

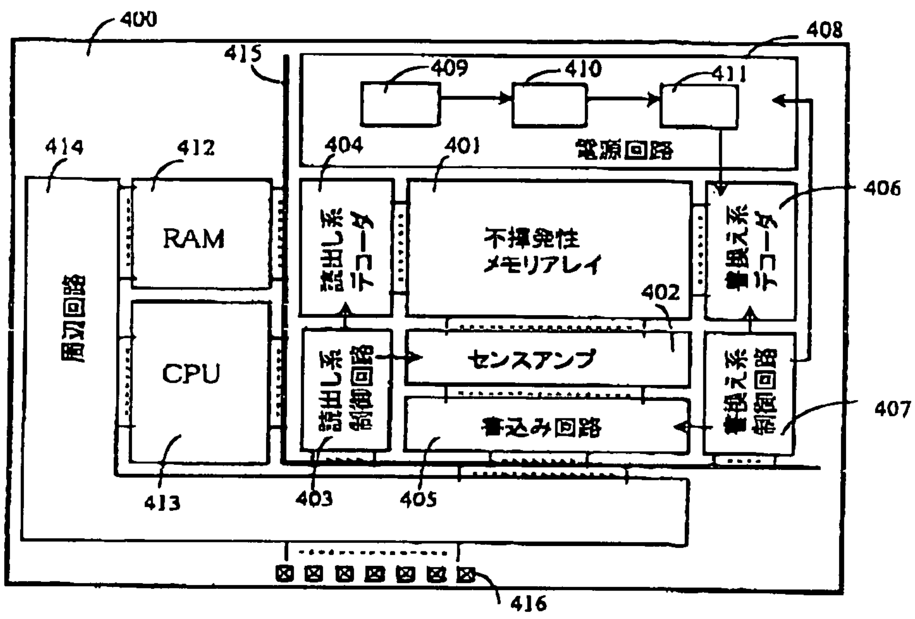
367: ELECTRODES OF PACKAGE INCORPORATING SECOND FIRST DEVICE (CONTROL BUS TERMINALS AND CONTROL TERMINALS OF FIRST DEVICE)

368: SOCKET IN WHICH NTH FIRST PACKET IS INSERTED

366: PACKAGE INCORPORATING NTH FIRST DEVICE

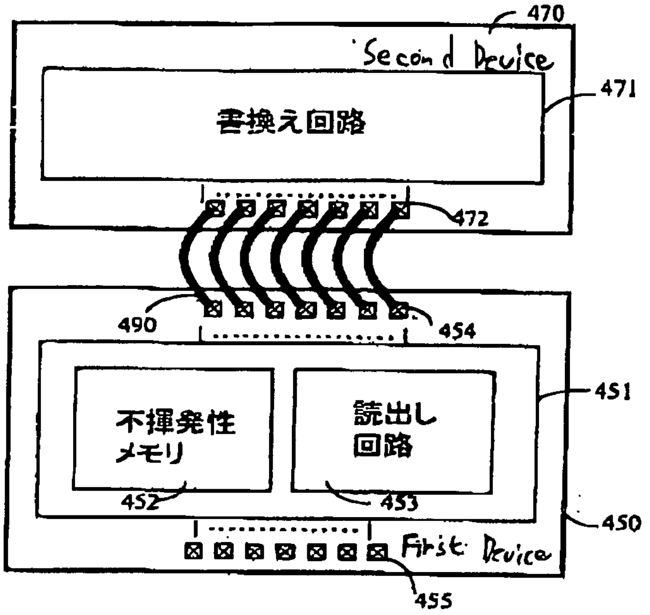
367: ELECTRODES OF PACKAGE INCORPORATING NTH FIRST DEVICE (CONTROL BUS TERMINALS AND CONTROL TERMINALS OF FIRST DEVICE)

Fig.12


400
415
408
409
410
411
電源回路
414
412
404
401
406
RAM
読出し系デコーダ
不揮発性メモリアレイ
書換え系デコーダ
402
周辺回路
CPU
読出し系制御回路
センスアンプ
書込み回路
書換え系制御回路
407
413
403
405
416

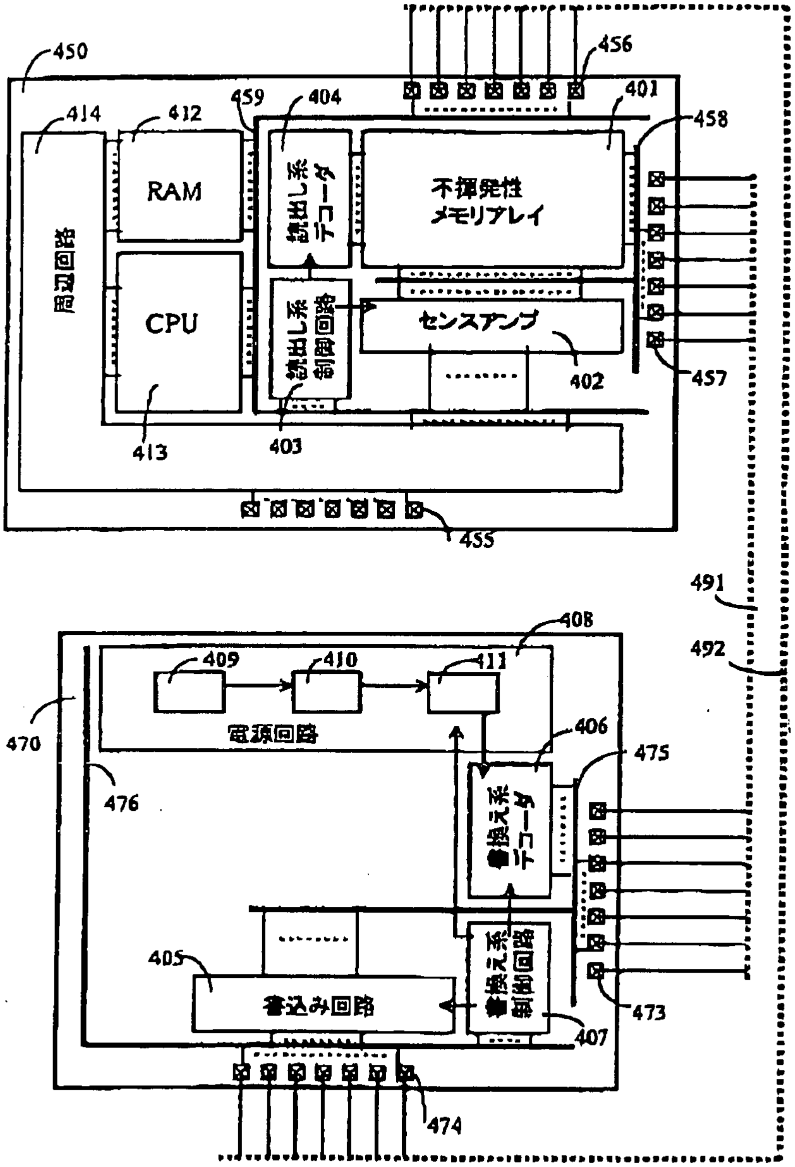
400: NONVOLATILE-MEMORY-INCORPORATED MICROCOMPUTER
401: NONVOLATILE MEMORY CELL ARRAY
402: SENSE AMPLIFIER CIR.
403: READING CONTROL CIR.
404: READING DECODER
405: WRITING CIR. (PAGE LATCH)
406: REWRITING DECODER
407: REWRITING CONTROL CIR.
408: POWER CIR.
409: REFERENCE VOLTAGE TRIMMING CIR.
410: REFERENCE VOLTAGE GENERATION CIR.
411: REWRITING VOLTAGE GENERATION CIR.
414: PERIPHERAL CIRCUITS
415: CONTROL BUS
416: MICROCOMPUTER CONTROL TERMINAL

Fig.13


470
Second Device
471
書換え回路
472
490
454
451
不揮発性
メモリ
読出し
回路
452
453
450
First Device
455

450: SEMICONDUCTOR DEVICE (FIRST DEVICE) EXCLUDING NON-ALWAYS-USED PARTICULAR FUNCTION BLOCK
451: READ-ONLY NONVOLATILE MEMORY BLOCK
452: NONVOLATILE MEMORY
453: READING CIR.
454: REWRITING CONTROL BUS TERMINAL
455: CONTROL TERMINAL OF FIRST DEVICE
470: FIRST DEVICE REWRITING DEVICE (SECOND DEVICE)
471: FIRST DEVICE REWRITING CIR.
472: REWRITING CONTROL BUS TERMINAL
490: REWRITING SIGNAL LINE (CONNECTED ONLY AT THE TIME OF REWRITING)

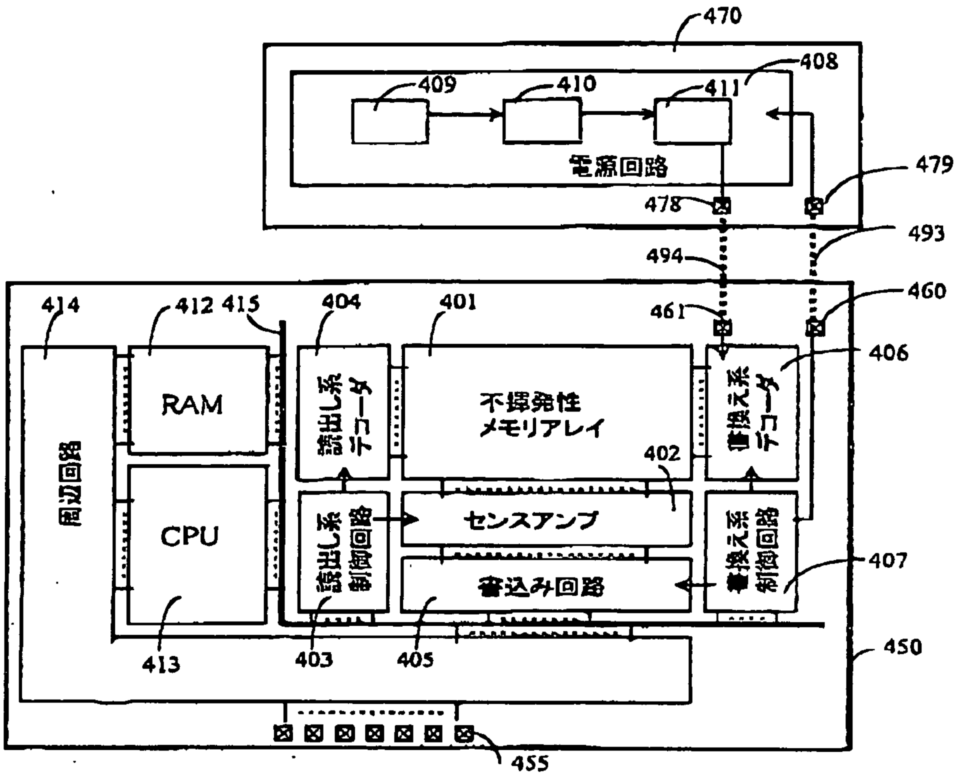
Fig. 14


450
414
412
459
404
401
456
458
RAM
CPU
周辺回路
読出し系デコーダ
不揮発性メモリアレイ
読出し系制御回路
センスアンプ
402
457
413
403
455
491
492
408
409
410
411
電源回路
406
475
470
476
書換え系デコーダ
書換え系制御回路
書込み回路
405
407
473
474

401: NONVOLATILE MEMORY CELL ARRAY
402: SENSE AMPLIFIER CIR.
403: READING CONTROL CIR.
404: READING DECODER
405: WRITING CIR. (PAGE LATCH)
406: REWRITING DECODER
407: REWRITING CONTROL CIR.
408: POWER CIR.
409: REFERENCE VOLTAGE TRIMMING CIR.
410: REFERENCE VOLTAGE GENERATION CIR.
411: REWRITING VOLTAGE GENERATION CIR.
414: PERIPHERAL CIRCUITS
450: MICROCOMPUTER INCORPORATING READ-ONLY NONVOLATILE MEMORY
(FIRST DEVICE)
455: CONTROL TERMINAL OF FIRST DEVICE
456: REWRITING CONTROL CONNECTION TERMINAL GROUP
457: REWRITING SIGNAL CONNECTION TERMINAL GROUP
458: REWRITING CONTROL BUS
459: CONTROL BUS
470: DEVICE (SECOND DEVICE) FOR REWRITING NONVOLATILE MEMORY O
FIRST DEVICE
473: REWRITING SIGNAL CONNECTION TERMINAL GROUP
474: REWRITING CONTROL CONNECTION TERMINAL GROUP
475: REWRITING CONTROL BUS
476: CONTROL BUS

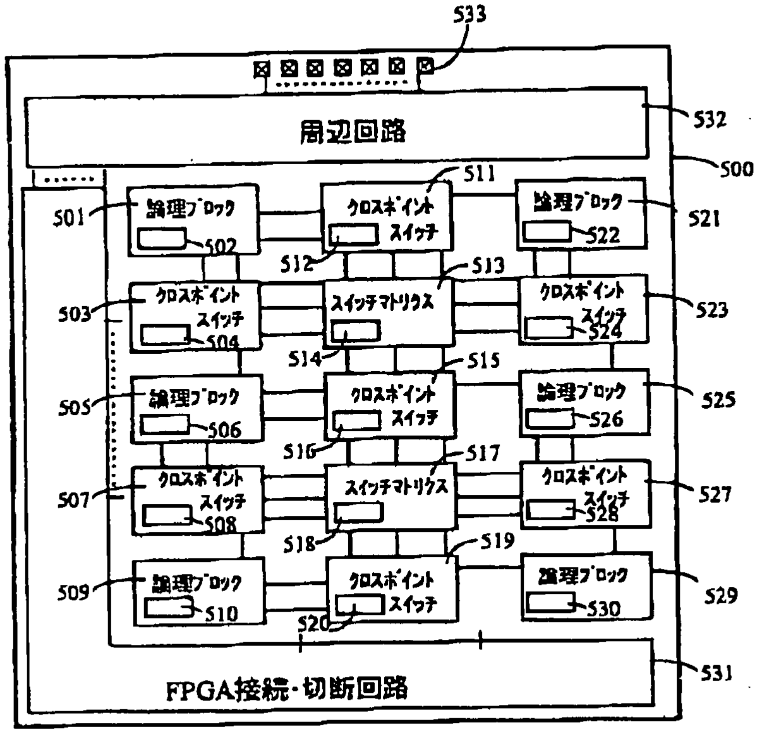
491: REWRITING BUS SIGNAL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF REWRITING)
492: BUS CONNECTION LINE (CONNECTED ONLY AT THE TIME OF REWRITING)

Fig. 15


470
408
409
410
411
電源回路
479
478
493
494
460
461
406
414
412
415
404
401
RAM
読出し系デコーダ
不揮発性メモリアレイ
書換え系デコーダ
周辺回路
402
CPU
読出し系制御回路
センスアンプ
書換え系制御回路
書込み回路
407
413
403
405
450
455

401: NONVOLATILE MEMORY CELL ARRAY
402: SENSE AMPLIFIER CIR.
403: READING CONTROL CIR.
404: READING DECODER
405: WRITING CIR. (PAGE LATCH)
406: REWRITING DECODER
407: REWRITING CONTROL CIR.
408: POWER CIR.
409: REFERENCE VOLTAGE TRIMMING CIR.
410: REFERENCE VOLTAGE GENERATION CIR.
411: REWRITING VOLTAGE GENERATION CIR.
414: PERIPHERAL CIRCUITS
415: CONTROL BUS
450: MICROCOMPUTER INCORPORATING READ-ONLY NONVOLATILE MEMORY (FIRST DEVICE)
455: CONTROL TERMINAL OF FIRST DEVICE
460: REWRITING CONTROL TERMINAL
461: REWRITING POWER CONNECTION TERMINAL
470: POWER DEVICE (SECOND DEVICE) FOR REWRITING NONVOLATILE MEMORY OF FIRST DEVICE
478: REWRITING POWER CONNECTION TERMINAL
479: REWRITING CONTROL TERMINAL
493: REWRITING CONTROL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF REWRITING)
494: REWRITING POWER CONNECTION LINE (CONNECTED ONLY AT THE TIME OF REWRITING)

Fig. 16


533
周辺回路
532
500
501
論理ブロック
502
511
クロスポイントスイッチ
512
論理ブロック
521
522
503
クロスポイントスイッチ
504
513
スイッチマトリクス
514
クロスポイントスイッチ
523
524
505
論理ブロック
506
515
クロスポイントスイッチ
516
論理ブロック
525
526
507
クロスポイントスイッチ
508
517
スイッチマトリクス
518
クロスポイントスイッチ
527
528
509
論理ブロック
510
519
クロスポイントスイッチ
520
論理ブロック
529
530
FPGA接続・切断回路
531

500 FPGA
(Field Programmable Gate Array)

501,505,509,521,525,529 LOGIC BLOCK

502,506,510,522,526,530 LOGIC BLOCK SETTING MEMORY

503,507,511,515,519,523,527 CROSS POINT SWITCH

504,508,512,516,520,524,528 CROSS POINT SWITCH SETTING MEMORY

513, 517: SWITCH MATRIX

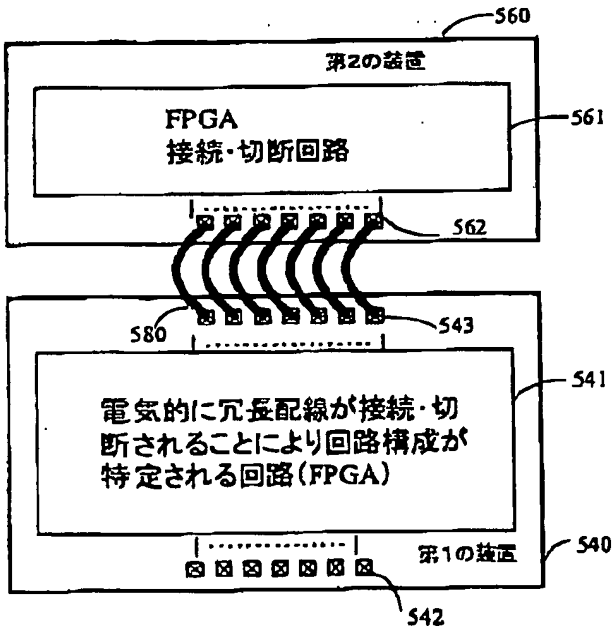
514, 518: SWITCH MATRIX SETTING MEMORY

531: FPGA CONNECTING/DISCONNECTING CIR.

532: PERIPHERAL CIRCUITS

533: FPGA CONTROL TERMINAL

Fig. 17


560
第2の装置
FPGA
接続・切断回路
561
562
580
543
541
電気的に冗長配線が接続・切断されることにより回路構成が特定される回路(FPGA)
第1の装置
540
542

540: DEVICE (FIRST DEVICE) THAT DOES NOT HAVE CONNECTING/DISCONNECTING FUNCTION AND WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY CONNECTING AND DISCONNECTING REDUNDANT WIRING ELECTRICALLY

541: CIRCUIT (FPGA) WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY CONNECTING AND DISCONNECTING REDUNDANT WIRING ELECTRICALLY

542: CONTROL TERMINAL OF FIRST DEVICE

543: CONNECTION/DISCONNECTION CONTROL TERMINAL

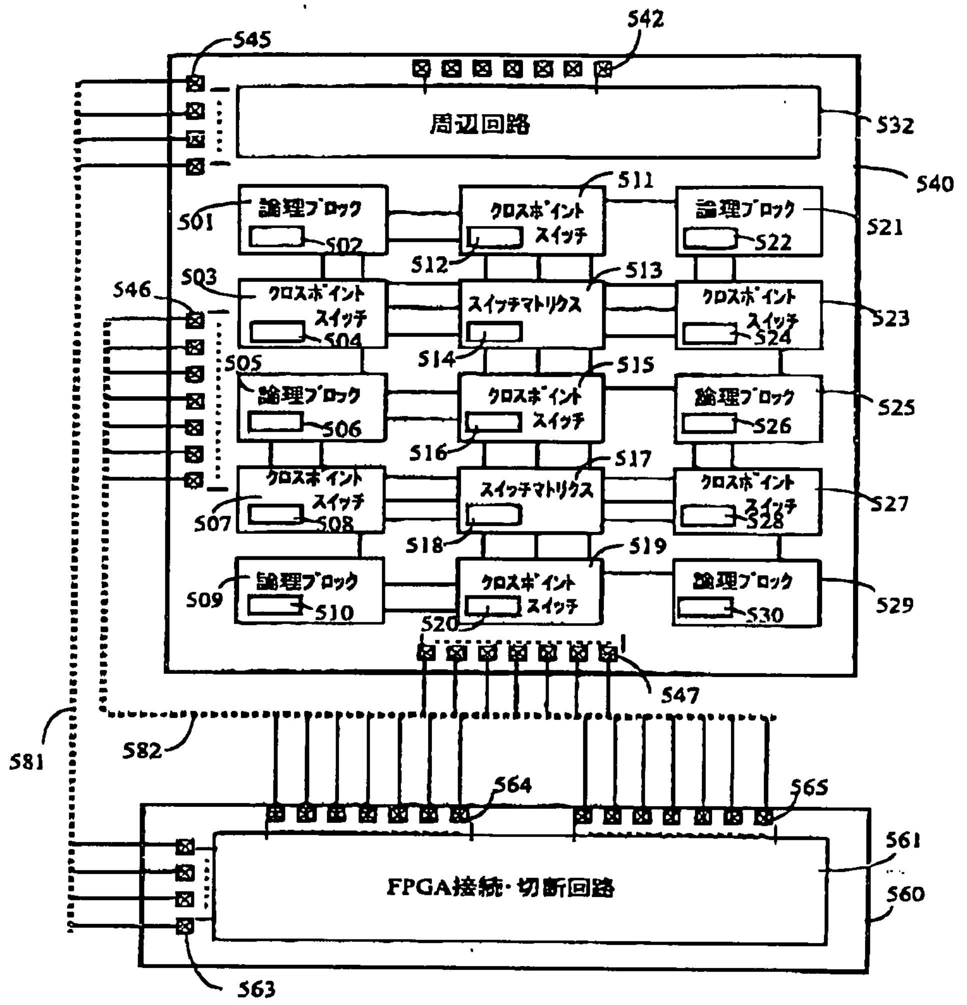
560: FIRST DEVICE CONNECTING/DISCONNECTING DEVICE (SECOND DEVICE)

561: FIRST DEVICE CONNECTING/DISCONNECTING CIR.

562: CONNECTION/DISCONNECTION CONTROL TERMINAL

580: CONNECTION/DISCONNECTION CONTROL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

Fig. 18



542
545
周辺回路
532
540
501
論理ブロック
502
511
クロスポイントスイッチ
512
論理ブロック
522
521
503
546
クロスポイントスイッチ
504
513
スイッチマトリクス
514
クロスポイントスイッチ
524
523
505
論理ブロック
506
515
クロスポイントスイッチ
516
論理ブロック
526
525
クロスポイントスイッチ
507
508
517
スイッチマトリクス
518
クロスポイントスイッチ
528
527
509
論理ブロック
510
519
クロスポイントスイッチ
520
論理ブロック
530
529
547
581
582
564
565
561
FPGA接続・切断回路
560
563

501, 505, 509, 521, 525, 529: LOGIC BLOCK

502, 506, 510, 522, 526, 530: LOGIC BLOCK SETTING MEMORY

503, 507, 511, 515, 519, 523, 527 CROSS POINT SWITCH

504, 508, 512, 516, 520, 524, 528 CROSS POINT SWITCH SETTING MEMORY

513, 517: SWITCH MATRIX

514, 518: SWITCH MATRIX SETTING MEMORY

532: PERIPHERAL CIRCUITS

540: DEVICE (FIRST DEVICE) THAT DOES NOT HAVE CONNECTING/DISCONNECTING FUNCTION AND WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY CONNECTING AND DISCONNECTING REDUNDANT WIRING ELECTRICALLY

542: CONTROL TERMINAL OF FIRST DEVICE

545: CONNECTION/DISCONNECTION CONTROL TERMINAL

546, 547: CONNECTION/DISCONNECTION SIGNAL TERMINAL

560: FIRST DEVICE (FPGA) CONNECTING/DISCONNECTING DEVICE (SECOND DEVICE)

561: FIRST DEVICE CONNECTING/DISCONNECTING CIR.

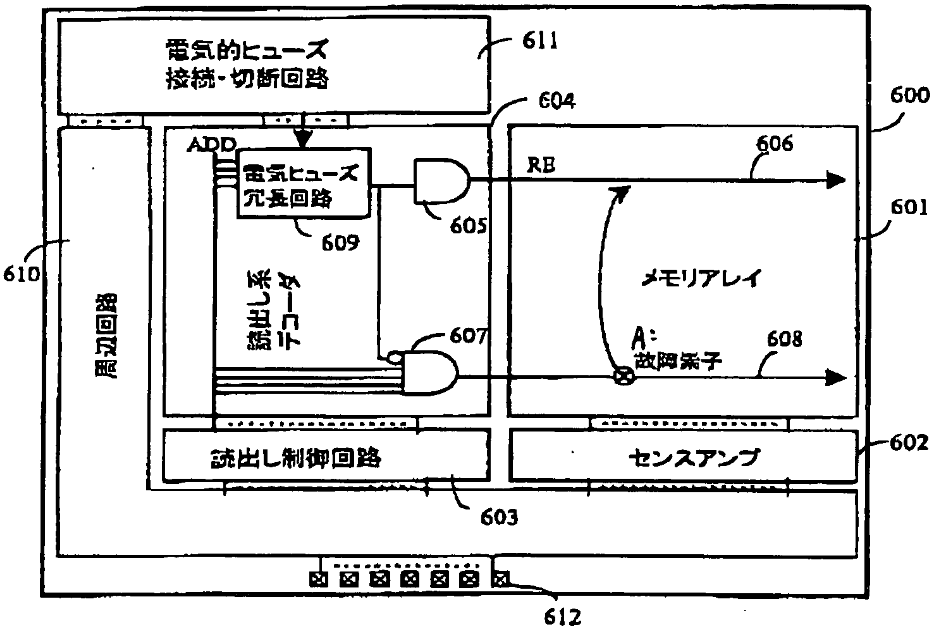
563: CONNECTION/DISCONNECTION CONTROL TERMINAL

564, 565: CONNECTION/DISCONNECTION SIGNAL TERMINAL

581: CONNECTION/DISCONNECTION CONTROL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

582: CONNECTION/DISCONNECTION SIGNAL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

Fig. 19

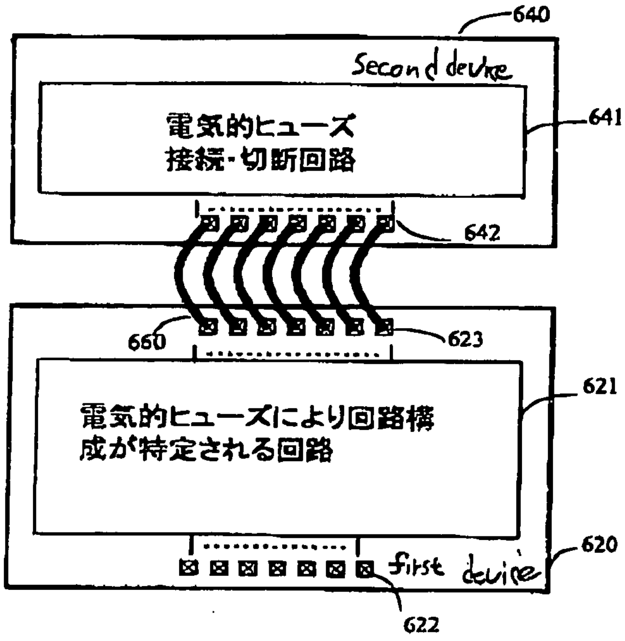


電気的ヒューズ
接続・切断回路
611
604
600
ADD
電気ヒューズ
冗長回路
RB
606
601
605
609
610
読出し系
デコーダ
周辺回路
メモリアレイ
607
A:
故障素子
608
読出し制御回路
センスアンプ
602
603
612

A: FAULTY ELEMENT

600: CIRCUIT WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRIC FUSES
601: MEMORY ARRAY
602: SENSE AMPLIFIER CIR.
603: READING CONTROL CIR.
604: READING DECODER
605: REDUNDANT DECODER
606: REDUNDANT WORD LINE
607: DECODER
608: WORD LINE
609: ELECTRIC FUSE REDUNDANT CIR.
610: PERIPHERAL CIRCUITS
611: ELECTRIC FUSE CONNECTING/DISCONNECTING CIR.
612: CONTROL TERMINAL OF SEMICONDUCTOR DEVICE

Fig. 20


640
Second device
641
電気的ヒューズ
接続・切断回路
642
660
623
621
電気的ヒューズにより回路構
成が特定される回路
620
first device
622

620: DEVICE (FIRST DEVICE) THAT DOES NOT HAVE CONNECTING/DISCONNECTING FUNCTION AND WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRIC FUSES

621: CIRCUIT WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRIC FUSES

622: CONTROL TERMINAL OF FIRST DEVICE

623: CONNECTION/DISCONNECTION CONTROL TERMINAL

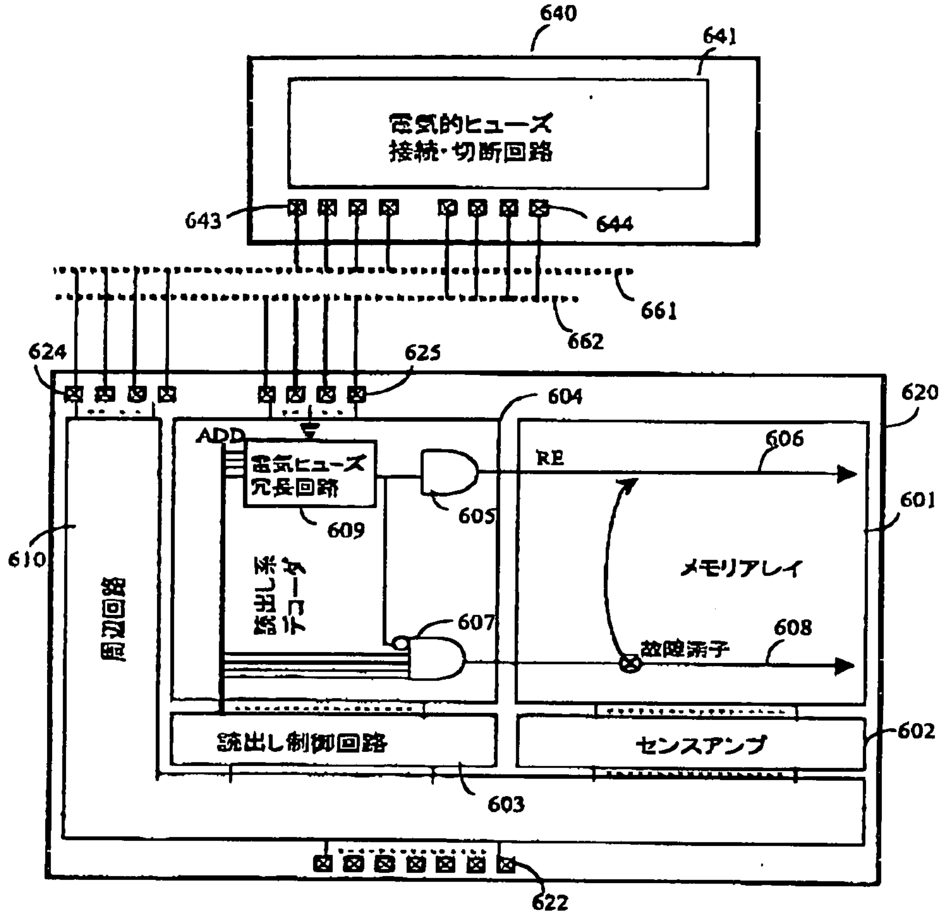
640: FIRST DEVICE CONNECTING/DISCONNECTING DEVICE (SECOND DEVICE)

641: FIRST DEVICE CONNECTING/DISCONNECTING CIR.

642: CONNECTION/DISCONNECTION CONTROL TERMINAL

660: CONNECTION/DISCONNECTION CONTROL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

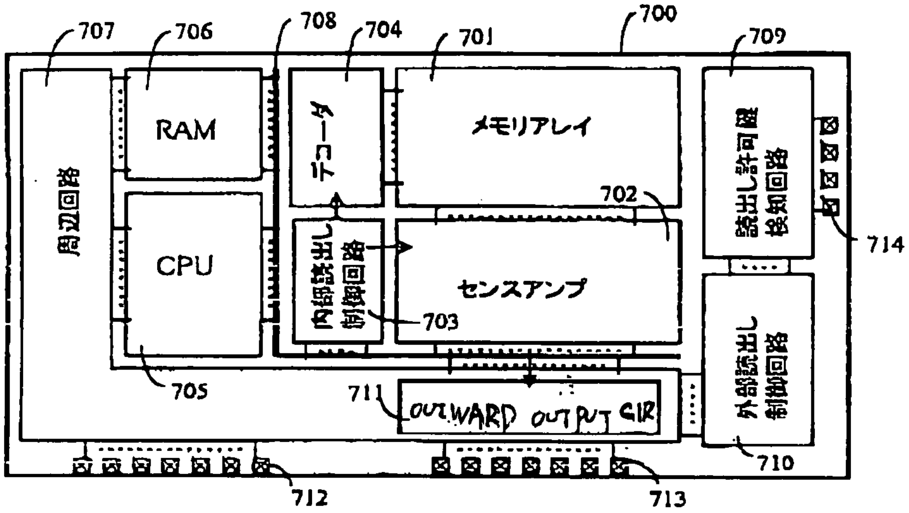
Fig.21


640
641
電気的ヒューズ
接続・切断回路
643
644
661
662
624
625
604
620
ADD
電気ヒューズ
冗長回路
RE
606
605
609
601
610
周辺回路
読出し系
デコーダ
メモリアレイ
607
608
故障素子
読出し制御回路
センスアンプ
602
603
622

A: FAULTY ELEMENT

601: MEMORY ARRAY
602: SENSE AMPLIFIER CIR.
603: READING CONTROL CIR.
604: READING DECODER
605: REDUNDANT DECODER
606: REDUNDANT WORD LINE
607: DECODER
608: WORD LINE
609: ELECTRIC FUSE REDUNDANT CIR.
610: PERIPHERAL CIRCUITS
620: DEVICE (FIRST DEVICE) THAT DOES NOT HAVE CONNECTING/DISCONNECTING FUNCTION AND WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRIC FUSES
622: CONTROL TERMINAL OF FIRST DEVICE
624: CONNECTION/DISCONNECTION CONTROL TERMINAL
625: CONNECTION/DISCONNECTION SIGNAL TERMINAL
640: DEVICE (SECOND DEVICE) FOR CONNECTING AND DISCONNECTING ELECTRIC FUSES OF FIRST DEVICE
641: DEVICE FOR CONNECTING AND DISCONNECTING ELECTRIC FUSES OF FIRST DEVICE
643: CONNECTION/DISCONNECTION CONTROL TERMINAL
644: CONNECTION/DISCONNECTION SIGNAL TERMINAL
661: CONNECTION/DISCONNECTION CONTROL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)
662: CONNECTION/DISCONNECTION SIGNAL CONNECTION LINE (CONNECTED ONLY WHEN CONNECTIONS AND DISCONNECTIONS ARE MADE)

Fig.22

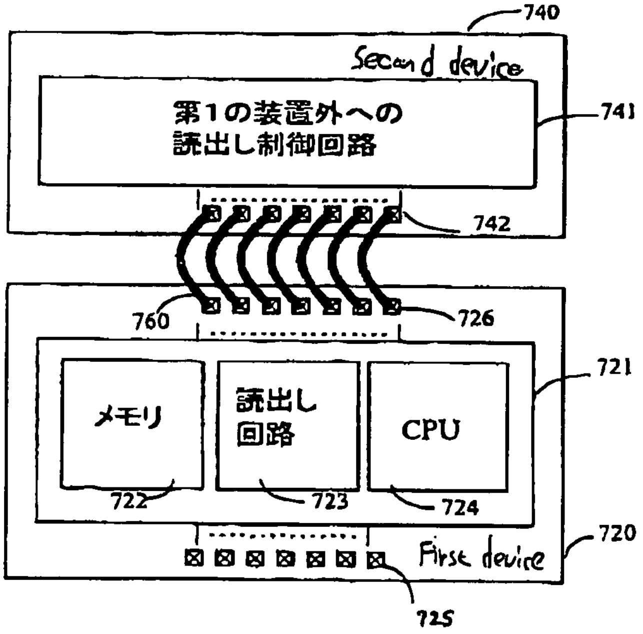


707
706
708
704
701
700
709
RAM
周辺回路
デコーダ
メモリアレイ
読出し許可鍵検知回路
702
CPU
内部読出し制御回路
センスアンプ
714
703
外部読出し制御回路
705
711
OUTWARD OUTPUT CIR
710
712
713

700: MICROCOMPUTER
701: MEMORY ARRAY
702: SENSE AMPLIFIER CIR.
703: MICROCOMPUTER INTERNAL READING CONTROL CIR.
704: READING DECODER
707: PERIPHERAL CIRCUITS

708: CONTROL BUS
709: READING PERMISSION KEY DETECTION CIR.
710: OUTWARD READING CONTROL CIR.
711: OUT-OF-MICROCOMPUTER OUTPUT CIR.
712: MICROCOMPUTER CONTROL TERMINAL
713: MEMORY DATA OUTPUT TERMINAL
714: READING PERMISSION KEY INPUT TERMINAL

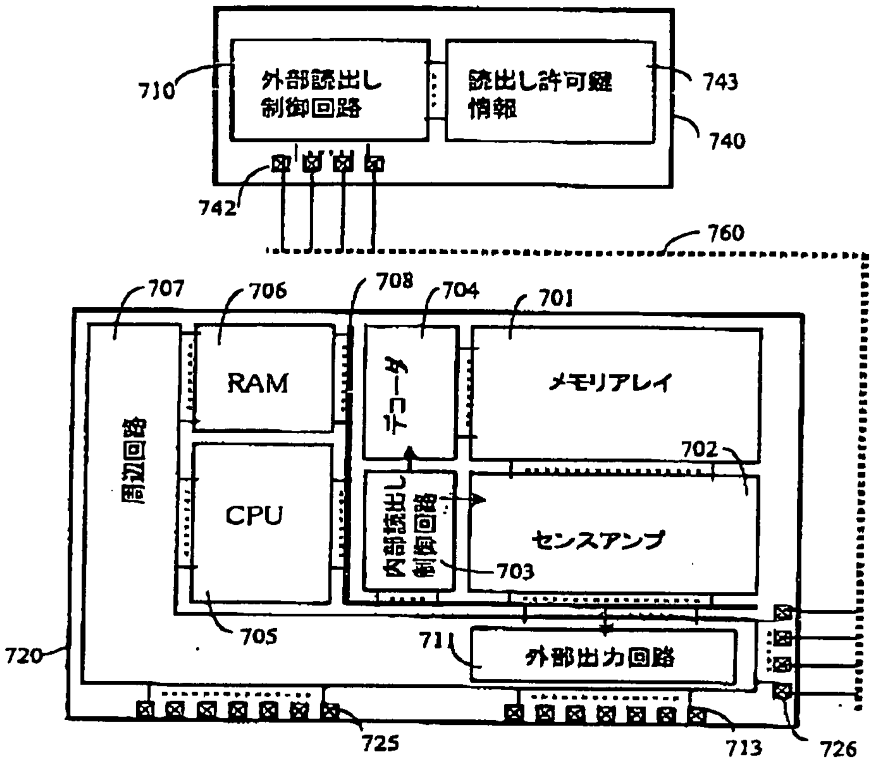
Fig.23



740
Second device
第1の装置外への読出し制御回路
741
742
760
726
721
メモリ
読出し回路
CPU
722
723
724
720
First device
725

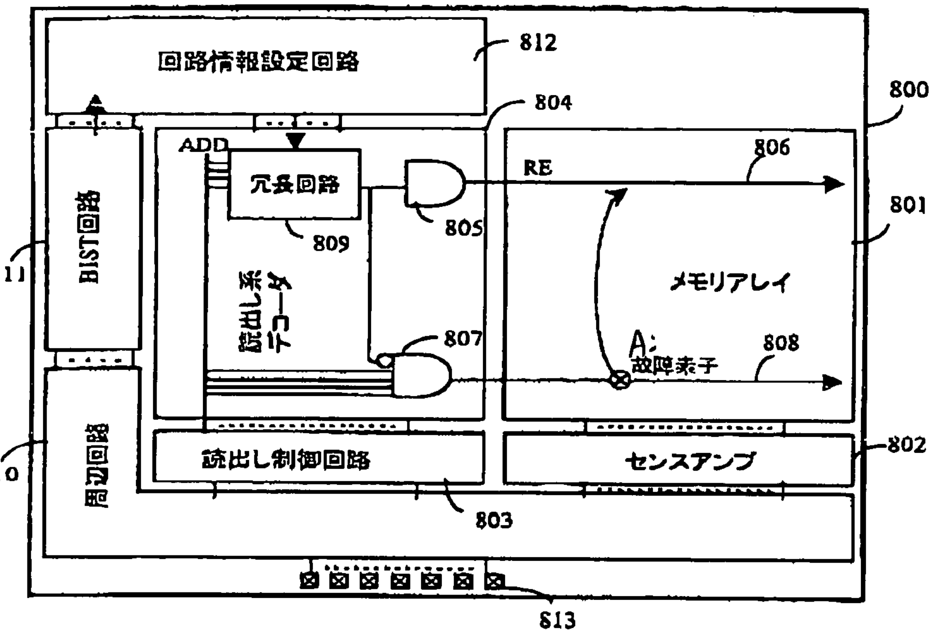
720: MICROCOMPUTER (FIRST DEVICE) NOT HAVING OUT-OF-CHIP MEMORY DATA READING FUNCTION
721: CIRCUIT CAPABLE OF READING MEMORY DATA ONLY INSIDE CHIP
722: MEMORY
723: MICROCOMPUTER INTERNAL READING CIR.
725: CONTROL TERMINAL OF FIRST DEVICE
726: OUTWARD READING CONTROL TERMINAL
740: OUT-OF-FIRST-DEVICE READING CONTROL DEVICE (SECOND DEVICE)
741: OUT-OF-FIRST-DEVICE READING CONTROL CIR.
742: OUTWARD READING CONTROL TERMINAL
760: OUTWARD READING CONTROL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF OUT-OF-CHIP READING)

Fig.24


外部読出し制御回路
読出し許可鍵情報
710
743
740
742
760
707
706
708
704
701
RAM
デコーダ
メモリアレイ
周辺回路
702
CPU
内部読出し制御回路
センスアンプ
703
705
711
外部出力回路
720
725
713
726

701: MEMORY ARRAY
702: SENSE AMPLIFIER CIR.
703: MICROCOMPUTER INTERNAL READING CONTROL CIR.
704: READING DECODER
707: PERIPHERAL CIRCUITS
708: CONTROL BUS
710: OUTWARD READING CONTROL CIR.
711: OUT-OF-MICROCOMPUTER OUTPUT CIR.
713: MEMORY DATA OUTPUT TERMINAL
720: MICROCOMPUTER (FIRST DEVICE) NOT HAVING OUT-OF-DEVICE MEMORY DATA READING FUNCTION
725: CONTROL TERMINAL OF FIRST DEVICE
726: OUTWARD READING CONTROL TERMINAL
740: OUT-OF-FIRST-DEVICE READING CONTROL DEVICE (SECOND DEVICE)
742: OUTWARD READING CONTROL TERMINAL
743: OUT-OF-FIRST-DEVICE READING PERMISSION KEY INFORMATION
760: OUTWARD READING CONTROL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF OUT-OF-DEVICE READING)
]

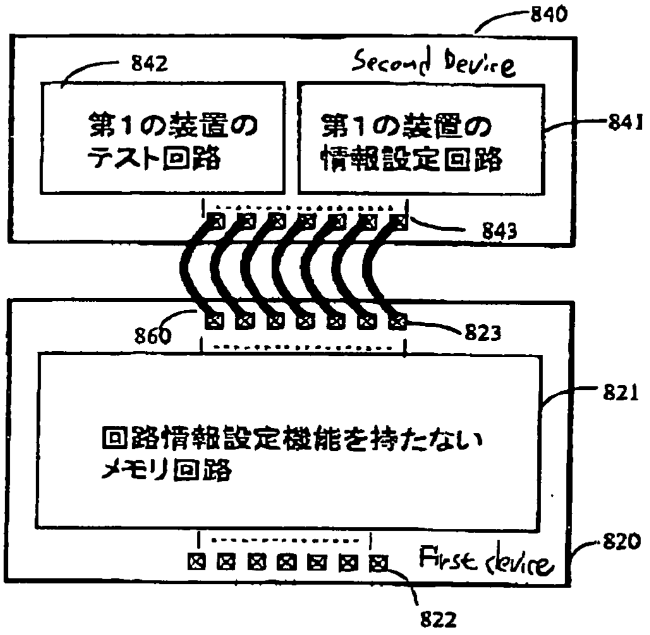
Fig. 25


回路情報設定回路
812
800
804
ADD
冗長回路
RE
806
801
BIST回路
809
805
811
メモリアレイ
読出し系デコーダ
807
A:
故障素子
808
読出し制御回路
センスアンプ
802
810
周辺回路
803
813

A: FAULTY ELEMENT

800: CIRCUIT IN WHICH CIRCUIT INFORMATION CAN BE SET ON THE BASIS OF BIST (BUILT-IN SELF-TEST) RESULTS
801: MEMORY ARRAY
802: SENSE AMPLIFIER CIR.
803: READING CONTROL CIR.
804: READING DECODER
805: REDUNDANT DECODER
806: REDUNDANT WORD LINE
807: DECODER
808: WORD LINE
809: REDUNDANT CIR.
810: PERIPHERAL CIRCUITS
811: BIST (BUILT-IN SELF-TEST) CIR.
812: CIRCUIT INFORMATION SETTING CIR.
813: SEMICONDUCTOR DEVICE CONTROL TERMINAL

Fig.26


840
842
Second Device
第1の装置の
テスト回路
第1の装置の
情報設定回路
841
843
860
823
821
回路情報設定機能を持たない
メモリ回路
820
First device
822

820: DEVICE NOT HAVING CIRCUIT INFORMATION SETTING FUNCTION (FIRST DEVICE)

821: CIRCUIT WHOSE CIRCUIT CONFIGURATION IS DETERMINED BY ELECTRICAL INFORMATION

822: CONTROL TERMINAL OF FIRST DEVICE

823: CIRCUIT INFORMATION SETTING TERMINAL

840: TESTING AND INFORMATION SETTING DEVICE (SECOND DEVICE) FOR FIRST DEVICE

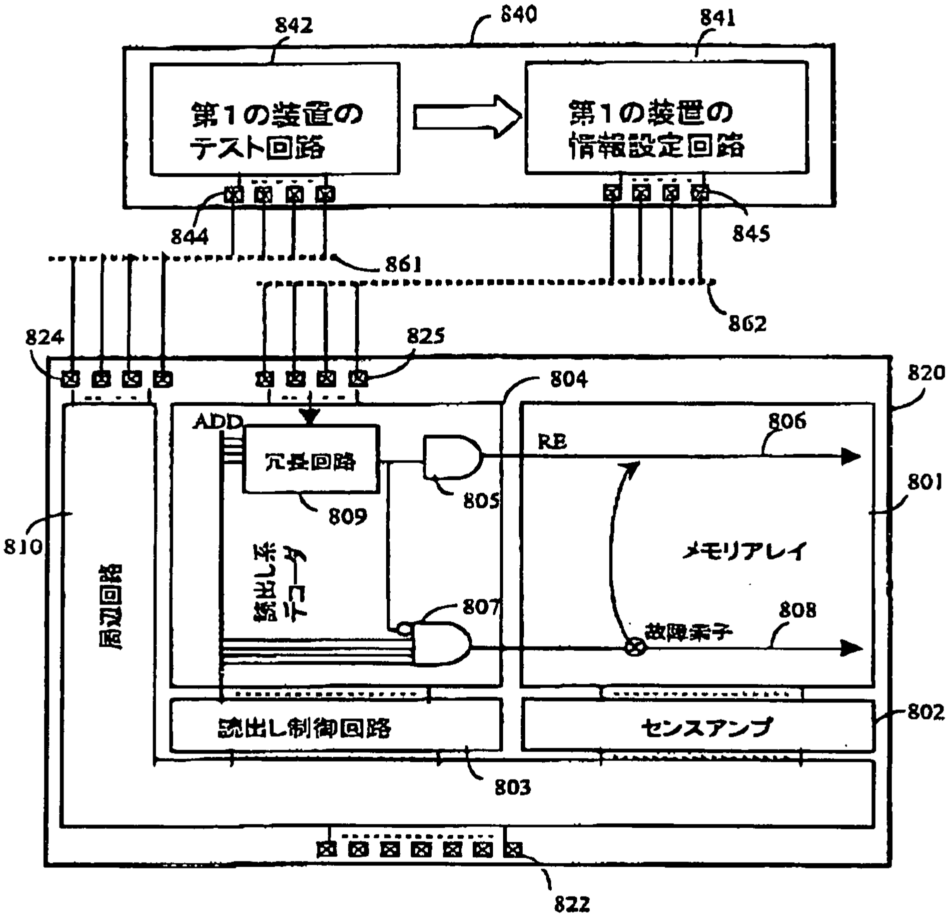
841: INFORMATION SETTING CIR. FOR FIRST DEVICE

842: TESTING CIR. FOR FIRST DEVICE

843: CIRCUIT INFORMATION SETTING TERMINAL

860: INFORMATION SETTING SIGNAL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF INFORMATION SETTING)

Fig.27



842
840
841
第1の装置のテスト回路
第1の装置の情報設定回路
844
845
861
862
824
825
804
820
ADD
冗長回路
806
RE
801
805
809
810
周辺回路
読出し系デコーダ
メモリアレイ
807
808
故障素子
読出し制御回路
センスアンプ
802
803
822

801: MEMORY ARRAY
802: SENSE AMPLIFIER CIR.
803: READING CONTROL CIR.
804: READING DECODER
805: REDUNDANT DECODER
806: REDUNDANT WORD LINE
807: DECODER
808: WORD LINE
809: REDUNDANT CIR.
810: PERIPHERAL CIRCUITS

820: DEVICE NOT HAVING CIRCUIT INFORMATION SETTING FUNCTION (FIRST DEVICE)
822: CONTROL TERMINAL OF FIRST DEVICE
824: TESTING AND CIRCUIT INFORMATION SETTING CONTROL TERMINAL
825: CIRCUIT INFORMATION SETTING TERMINAL
840: TESTING AND INFORMATION SETTING DEVICE (SECOND DEVICE) FOR FIRST DEVICE
841: INFORMATION SETTING CIR. FOR FIRST DEVICE
842: TESTING CIR. FOR FIRST DEVICE
844: TESTING AND CIRCUIT INFORMATION SETTING CONTROL TERMINAL
845: CIRCUIT INFORMATION SETTING TERMINAL
861: INFORMATION SETTING CONTROL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF INFORMATION SETTING)
862: INFORMATION SETTING SIGNAL CONNECTION LINE (CONNECTED ONLY AT THE TIME OF INFORMATION SETTING)